

# METHOD OF MANUFACTURING FLASH MEMORY DEVICE

## BACKGROUND OF THE INVENTION

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### Field of the Invention:

The invention relates generally to a method of manufacturing a flash memory device. More particularly, the invention relates to a method of manufacturing a flash memory device capable of reducing the effective thickness of a dielectric film, in a way that a lower oxide film is formed and the dielectric film consisting of the lower oxide film, a nitride film and an upper oxide film is then formed by implementing a nitrification process and oxygen annealing process.

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### Description of the Prior Art:

Currently, an ONO film is usually used as a dielectric film of a high-integration flash memory device of over  $0.18\mu\text{m}$ , which consists of a lower oxide film( $\text{SiO}_2$ ), a nitride film( $\text{Si}_3\text{N}_4$ ) and an upper oxide film( $\text{SiO}_2$ ). The ONO film has the effective thickness of about  $100\text{\AA}$ . In addition, if the thickness of the ONO film is reduced within the range in which the insulating breakage strength characteristic of a gate oxide film is not degraded, the ONO film can be used for a low voltage device. The gate of the flash memory cell can be effectively controlled by even low voltage.

The ONO film serves as a barrier for preventing loss of electrons into a

control ate in the floating gate. In order to perform this barrier, a thermal oxide film is most suitable. As the first polysilicon film used as the floating gate is crystallized and doped in-situ, however, the degree of oxidization in the grain and the grain boundary is different. As such, when the oxidization process is implemented, it is difficult to uniformly exactly control the thickness of a grown oxide film. Therefore, in a basic process today, a high temperature oxide film (HTO) deposited in thickness of about 40 Å by means of chemical vapor deposition(CVD) method using  $\text{SiH}_2\text{Cl}_2$ (DCS) gas, is used as the lower oxide film and the upper oxide film of the ONO film, respectively.

A  $\text{Si}_3\text{N}_4$  film deposited in thickness of about 50~60 Å by means of LPCVD method is used as the nitride film. Further, in order to stabilize the interface characteristic and remove the trap charges, a steam annealing process of a wet oxidization process is implemented.

As above, it is assumed that the entire thickness of the ONO film is important. As the design rule becomes small, there is a necessity to deposit the ONO film having a small effective rule. As the ONO film consists of three films, however, there is rarely reduction in the thickness and variations in the ratio. Thus, there is a limitation to reduce the thickness. Also, it is difficult to prohibit increase in the leakage current and decrease in the breakdown current.

## SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method of manufacturing a flash memory device capable of reducing the effective

thickness of a dielectric film.

Another object of the present invention is to provide a method of manufacturing a flash memory device capable of easily implementing a low voltage flash memory device by reducing the effective thickness of a dielectric film.

In order to accomplish the above object, a method of manufacturing a flash memory device according to the present invention is characterized in that it comprises the steps of sequentially forming a tunnel oxide film and a first polysilicon film on a semiconductor substrate and then etching the first polysilicon film and a given region of the tunnel oxide film; forming a lower oxide film on the entire structure; performing a nitrification process to form a nitrogen layer below the lower oxide film; performing an annealing process using an oxygen gas so that the nitrogen layer is moved on the surface of the lower oxide film, thus forming a nitride film; forming an upper oxide film on the entire surface to form a dielectric film consisting of the lower oxide film, the nitride film and the upper oxide film; sequentially forming a second polysilicon film, a tungsten silicide film and an anti-reflection film on the entire structure; and patterning the anti-reflection film, the tungsten silicide film, the second polysilicon film and the dielectric film to form a control gate, and then patterning the first polysilicon film and the tunnel oxide film to form a floating gate.

The lower oxide film is formed using DCS gas and  $N_2O$  or  $NO$  gas at the temperature of  $810 \sim 850^\circ C$  and is also formed in thickness of  $35 \sim 100 \text{ \AA}$  at the deposition rate of  $4 \sim 10 \text{ \AA/min}$ .

The nitrification process is performed by introducing  $\text{N}_2\text{O}$  or  $\text{NO}$  of 1  
~ 20ℓ into the furnace at the temperature of 810 ~ 850℃ for 10 ~ 20  
minutes so that the nitrogen film can have the thickness of 3 ~ 5 Å. The  
annealing process using the oxygen gas is performed by introducing an oxygen  
5 gas of 5 ~ 20ℓ into the furnace at the temperature of 850 ~ 950℃ for 5 ~ 20  
minutes.

The upper oxide film is formed using DCS gas and  $\text{N}_2\text{O}$  or  $\text{NO}$  gas at  
the temperature of 810 ~ 850℃ and is also formed in thickness of 35 ~ 100 Å  
at the deposition rate of 4 ~ 10 Å/min.

10 The second polysilicon film is formed in a double structure of a doped  
polysilicon film and an undoped polysilicon film, the polysilicon film and the  
undoped polysilicon film is deposited at the ratio of 4:1 ~ 7:1.

## BRIEF DESCRIPTION OF THE DRAWINGS

15 The aforementioned aspects and other features of the present invention  
will be explained in the following description, taken in conjunction with the  
accompanying drawings, wherein:

Figs 1A through 1E are cross-sectional views of a flash memory device,  
which are sequentially shown in order to explain a method of manufacturing  
20 the device according to the present invention;

Fig. 2 is a process chart illustrating the detailed condition for forming a  
dielectric film of the flash memory device according to the present invention;  
and

Figs. 3A and 3B illustrate the concentration distribution of nitrogen

after a lower oxide film is nitrified and an oxygen annealing process is performed, according to the present invention.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

5 The present invention will be described in detail by way of a preferred embodiment with reference to accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

Figs 1A through 1E are cross-sectional views of a flash memory device, which are sequentially shown in order to explain a method of manufacturing the device according to the present invention.

Referring now to Fig. 1A, a device isolation film 102 is formed at a given region of a semiconductor substrate 101 to define an active region and a device isolation region. An impurity ion implantation process is performed on the semiconductor substrate 101 of the defined active region to form a well region (not shown). Then, a tunnel oxide film 103 and a first polysilicon film 104 are sequentially formed on the entire structure. The first polysilicon film 104 and a given region of the tunnel oxide film 103 are etched by means of photolithography using the first mask and etching process. The semiconductor substrate 101 is cleaned before the tunnel oxide film 103 is formed. At this time, a mixed solution of HF and SC-1 in the ratio of 50:1 may be used or a mixed solution of BOE and SC-1 in the ratio of 100:1~300:1 may be used. In addition, the tunnel oxide film 103 is formed by performing wet oxidation process at the temperature of 750~800℃ and by performing annealing process at the temperature of 900~910℃ under

nitrogen ( $N_2$ ) atmosphere of  $5 \sim 10\ell$  for 20-30 minutes. As above, the interface defect density with semiconductor substrate 101 can be minimized since the tunnel oxide film 103 is formed by wet oxidation process. Meanwhile, the first polysilicon film 104 is formed at the temperature of  
5  $550 \sim 620^\circ\text{C}$  under the pressure of  $0.1 \sim 1\text{Torr}$  using  $\text{SiH}_4$  or  $\text{Si}_2\text{H}_6$  and  $\text{PH}_3$  gas. At this time, with the phosphorous (P) concentration of the first polysilicon film 104 being a high concentration of  $1.0\text{E}20 \sim 3.0\text{E}20$  atoms/cc, sufficient dopants are supplied in order to give the conductivity through diffusion and activation of phosphorous by means of a subsequent annealing  
10 process.

Referring now to Figs. 1B and 2, the wafer in which the tunnel oxide film 103 and the first polysilicon film 104 are formed is loaded into a reaction furnace in which the temperature of  $600 \sim 700^\circ\text{C}$  and  $N_2$  atmosphere of  $10 \sim 20\ell$  are kept (201 in Fig. 2). After the temperature of the furnace is  
15 raised at the  $N_2$  atmosphere of  $5 \sim 10\ell$  to  $810 \sim 850^\circ\text{C}$  (202 in Fig. 2), a lower oxide film 105 is deposited by means of LPCVD method using DCS and  $N_2\text{O}$  or NO gas (203 in Fig. 2). At this time, the lower oxide film 105 is deposited in thickness of  $35 \sim 100\text{\AA}$  at the deposition rate of  $4 \sim 10\text{\AA}/\text{min}$ . Also, with the temperature of the furnace kept at  $810 \sim 850^\circ\text{C}$ , introduction of DCS is  
20 stopped. Nitrification process by which  $N_2\text{O}$  or NO gas of  $1 \sim 20\ell$  is introduced for  $10 \sim 20$  minutes is then implemented (204 in Fig. 2). At this time, the thickness of the increasing lower oxide film 105 is about  $3 \sim 5\text{\AA}$ . The reason is that the nitrogen layer 106 is formed below the lower oxide film 105 as the nitrogen concentration distribution shown in Fig. 3A. In other

words, the nitrogen layer 106 is formed in thickness of 3~5Å below the lower oxide film 105.

Referring now to Figs. 1C and 2, after the nitrification process, a nitrogen purge process is implemented to raise the temperature of the furnace to 850~950°C under the N<sub>2</sub> atmosphere of 5~10ℓ (205 in Fig. 2). After the temperature within the furnace is raised, an annealing process is implemented by introducing an oxygen gas of about 5~20ℓ for 5~20 minutes (206 in Fig. 2). Thus, the surface of the first polysilicon film 104 is oxidized and the nitrogen layer 106 is therefore moved on a upper side of the lower oxide film 105, thus forming a nitride film 107, as shown in Fig. 3B.

By reference to Figs. 1D and 2, after the temperature within the furnace is decreased to 810~850°C under the N<sub>2</sub> atmosphere of 5~10 (207 in Fig. 2), an upper oxide film 108 is formed in thickness of 35~100Å by means of LPCVD method using DCS gas and N<sub>2</sub>O or NO gas (208 in Fig. 2). Then, after the temperature within the furnace is decreased to 600~700°C (209 in Fig. 2), the wafer in which the ONO dielectric film is formed is unloaded from the furnace (210 in Fig. 2).

Referring now to Fig. 1E, a second polysilicon film 109 and a tungsten silicide film 110 are sequentially formed on the entire structure and an anti-reflection film 111 is then formed. At this time, the second polysilicon film 109 is formed by means of LPCVD method at the temperature of 530~550°C under the pressure of 0.1~1Torr. Meanwhile, the second polysilicon film 109 may be formed in a double structure of a doped polysilicon film and an undoped polysilicon film. At this time, it is recommended that the deposition

ratio of the doped polysilicon film and the undoped polysilicon film is 4:1~7:1 and the entire thickness is 500~1000 Å. By doing this, when the tungsten silicide film 110 is deposited, diffusion of fluorine (F) that is solidified/substituted into the dielectric film and that can increase the thickness of the dielectric film can be prevented.

In case of forming the second polysilicon film in a double structure, the second polysilicon film is formed in-situ. The double structure can be formed as follows: the doped polysilicon film is first formed using SiH<sub>4</sub> or Si<sub>2</sub>H<sub>6</sub> and PH<sub>3</sub> gas, and the undoped polysilicon film is then formed by introducing only SiH<sub>4</sub> or Si<sub>2</sub>H<sub>6</sub> gas with introduction of PH<sub>3</sub> gas being stopped. Also, the tungsten silicide film 109 is formed enough to implement an adequate step coverage at the temperature of 300~500°C using the reaction of DCS and WF<sub>6</sub> that have a lower fluorine (F) content, a low post anneal stress and a good adhesive force, and to have the stoichiometric ratio of about 2.0~2.8 in order to minimize the sheet resistance. Also, the anti-reflection film 111 is formed of an oxidization nitride film or a nitride film. Thereafter, the anti-reflection film 111, the tungsten silicide film 110 and the second polysilicon film 109 are patterned by means of the photolithography process using the second mask to form a control gate. Then, the upper oxide film 108, the nitride film 107, the lower oxide film 105, the first polysilicon film 104 and the tunnel oxide film 103 are etched to form a floating gate. Thus, a stack gate in which the floating gate, the ONO dielectric film and the control gate are stacked is formed. Thereafter, an impurity ion implantation process is performed to form a source and a drain, thus completing a stack gate



type flash memory cell.

As can be understood from the above description with the present invention, as the thickness of the ONO film can be reduced, the gate can be effectively controlled and a low voltage flash memory device can be thus easily implemented. Also, it can be expected that the nitride film formed by oxygen annealing process has a low electron capture density compared to an existing ONO film formation process since the nitride film has a low nitrogen concentration file up within the lower oxide film. Due to this, the operating characteristic of the device can be improved. Further, as the dielectric film formation process and the steam anneal process are substituted with a single process, the cost is reduced and the productivity is also improved.

The present invention has been described with reference to a particular embodiment in connection with a particular application. Those having ordinary skill in the art and access to the teachings of the present invention will recognize additional modifications and applications within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications, and embodiments within the scope of the present invention.